REMARKS

Present Status of the Application

This is a full and timely response to the outstanding Final Office Action mailed on February 2, 2006. The Final Office Action rejected claims 39, 46-50 U.S.C.§ 102(b), as being anticipated by Voldman et al. (US Patent No.6,015,993). Applicants have amended claim to improve clarity. For at least the following reasons, Applicants respectfully submit claims 39, 46-50 are in proper condition for allowance and reconsideration of this application is respectfully requested.

Discussion of Office Action Rejections

The Final Office Action rejected claims 39, and 46-50 under 35 U.S.C. 102(b) as being anticipated by Voldman et al. US Patent 6,015,993, Applicants have amended claim 39 and hereby otherwise traverses this rejection. As such, Applicant submits that claims 39, and 46-50 are now in condition for allowance.

With respect to claim 39, as currently amended, recites in part:

> 39.A method of forming a non-gate diode of a SOI, comprising:
>
> ...forming a lightly doped region in the well region, the lightly doped region comprising neighboring lightly doped P-type and N-type regions;
>
> ....

Applicant submits that such a method of forming a non-gate diode of a SOI, as set forth in claim 39 as amended, is neither taught, disclosed, nor suggested by Voldman, or any of the other cited references, taken alone or in combination.

The present invention recited in independent claim 39 is, for example, supported by FIG. 9. The method of forming a non-gate diode of a SOI is disclosed. The lightly doped P-type region and lightly doped N-type region (Fig. 9, element 98a and 98b) are formed neighboring to each other. The description of "neighboring lightly doped P-type and N-type regions" in claim 39 means that the lightly doped P-type region and lightly doped N-type region are directly connected to each other, as shown in Fig. 9G.

Voldman teaches, in FIG. 7, a light doped n-type region 144 and a light doped p-type region 144.

However, Voldman fails to teach the neighboring lightly doped P-type and N-type regions that is required for the present invention, as set forth in claim 39. The light doped n-type region 144 and a light doped p-type region 144 of Voldman aren't formed neighboring to each other. Therefore, claim 39 as currently amended should not be considered as being anticipated by Voldman et al. US Patent 6,015,99 or any of the other cited references, taken alone or in combination, and is submitted as allowable.

With respect to claim 46, as original, recites in parts:

> 46. A method of forming a non-gate diode in a CMOS process, comprising:
>
> providing a substrate having a well region therein;

... forming a pair of second type doped regions located in the well region and **respectively** adjacent to the blocking isolation structure, wherein each second type doped region is separated from the first type doped region by the well.

Applicant submits that such a method of forming a non-gate diode of a SOI, as set forth in claim 46, is neither taught, disclosed, nor suggested by Voldman, or any of the other cited references, taken alone or in combination.

The present invention recited in independent claim 46 is, for example, supported by FIG. 7G. The method of forming a non-gate diode in a CMOS process is disclosed. The pair of second type doped regions (Fig 7G, N-type doped regions 216a and 216b) is formed adjacent to the blocking isolation structure respectively. The description of "forming a pair of second type doped regions located in the well region and **respectively** adjacent to the blocking isolation structure" in claim 46 means that one of the second type doped regions is adjacent to the blocking isolation structure, and the other second type doped regions is adjacent to the blocking isolation structure, too.

Voldman teaches, in FIG. 7, an n-type region 144 and n-type region 164.

However, Voldman fails to teach the pair of second type doped regions **respectively** adjacent to the blocking isolation structure that is required for the present invention, as set forth in claim 46. The n-type region 164 of Voldman isn't formed adjacent to the blocking isolation structure. Therefore, claim 46 should not be considered as being anticipated by Voldman et al. US Patent 6,015,99 or any of the other cited references, taken alone or in combination, and is submitted as allowable.

If independent claim 46 is allowable over the prior art of record, then its dependent claims 47-50 are allowable as a matter of law, because these dependent claims contain all features of their respective independent claim 46. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 39, 46-50 are in proper condition for allowance and an action to such effect is earnestly solicited. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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